Exhibit 1

Exhibit A
ACQIS's Preliminary Infringement Contentions for U.S. Patent No. 9,529,768
Sony PlayStation 4

The chart below identifies where each element of the asserted claims of U.S. Patent No. 9,529,768 ("'768 patent") is found in the Sony PlayStation 4 series console (all models of PlayStation 4, including the PlayStation 4 Slim (including but not limited to CUH-2xxx models), PlayStation 4 Pro (including but not limited to CUH-7xxx models), and PlayStation 4 (including but not limited to CUH-1xxx models), are accused and are collectively referred to herein as "PlayStation 4" and "Accused Products"). ACQIS contends that all PlayStation 4 series consoles made, used, tested, offered for sale, sold, or imported into the United States by Sony, that share the features detailed below with reference to various exemplary PlayStation 4 models, infringed at least claims 1, 2, 13, and 17 of the '768 patent in the manner charted herein. Specifically, all PlayStation 4 series consoles that include PCIe functionality infringed as set forth below.

This chart contains evidence relating to various PlayStation 4 models, including the PlayStation 4 Slim (CUH-2xxx), PlayStation 4 Pro (CUH-7xxx), and PlayStation 4 (CUH-1xxx), with emphasis on the PlayStation 4 Slim but including additional evidence regarding other models as well. The features of these products that are relevant to infringement are common across all PlayStation 4 models. ACQIS reserves the right to identify additional accused PlayStation 4 products based on information obtained in discovery.

ACQIS's contentions are not limited to the PCIe implementations discussed below. ACQIS does not possess information regarding the specific manner in which all of the Accused Products utilize PCIe functionality, beyond the uses discussed below. ACQIS contends that all implementations of PCIe in the Accused Products infringed for the reasons set forth herein. ACQIS reserves the right to supplement and/or amend its contentions to provide further specificity based on information obtained in discovery.

Claim Language	**Infringement Evidence**
1. A computer, comprising:	The PlayStation 4 is a computer running Orbis OS, a modified version of FreeBSD 9.0, as its operating system. https://www.extremetech.com/gaming/159476-ps4-runs-orbis-os-a-modified-version-of-freebsd-thats-similar-to-linux; https://en.wikipedia.org/wiki/PlayStation_4_system_software.

Exhibit A
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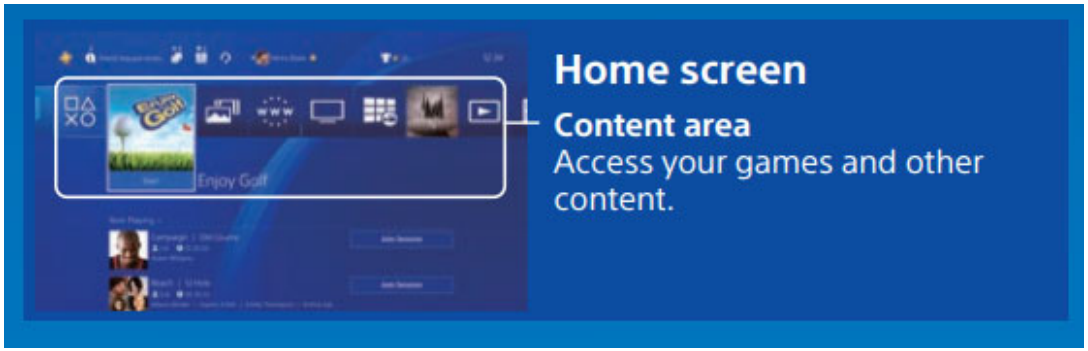
Sony PlayStation 4

Claim Language	Infringement Evidence
	 https://direct.playstation.com/en-us/consoles/console/playstation4-1tb-console.3003348.  https://manuals.playstation.net/document/pdf/CUH-2215A-5.5_1.pdf.

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ACQIS's Preliminary Infringement Contentions for U.S. Patent No. 9,529,768
Sony PlayStation 4

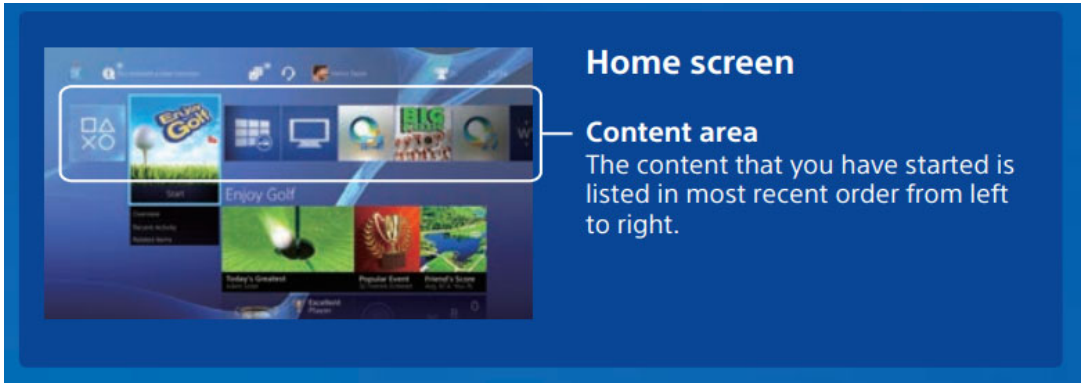
Claim Language	Infringement Evidence
	 https://manuals.playstation.net/document/pdf/CUH-1001A-1.5_1.pdf.
[1.a] an integrated central processing unit, interface controller and Phase-Locked Loop (PLL) clock circuitry in a single chip;	The PlayStation 4 contains an integrated central processing unit, interface controller and Phase-Locked Loop (PLL) clock circuitry in a single chip. The PlayStation 4 includes a Sony Interactive Entertainment Inc. (SIEI) single-chip custom processor, e.g., the CXD90059GB in the PlayStation 4 Slim, consisting of a CPU and GPU integrated on a single chip. All eight CPU cores and the GPU are on the same die.

Exhibit A
ACQIS's Preliminary Infringement Contentions for U.S. Patent No. 9,529,768
Sony PlayStation 4

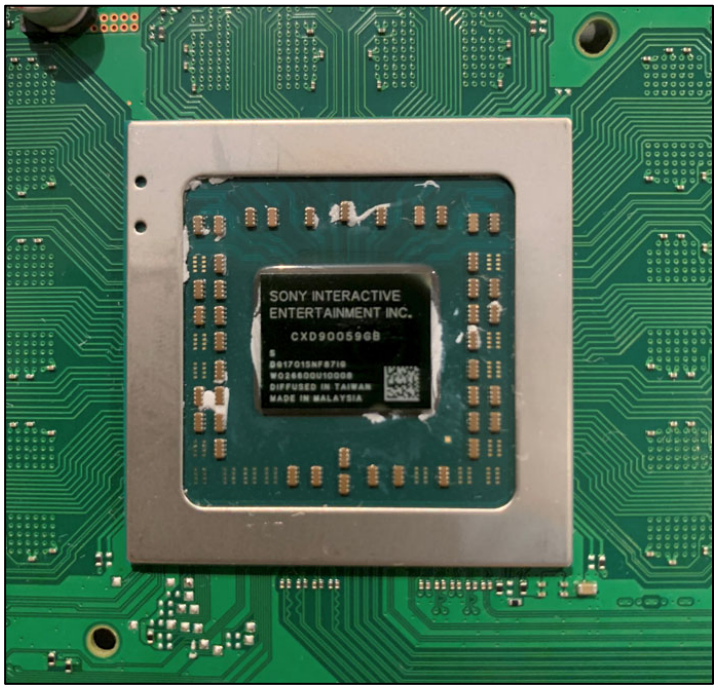
Claim Language	Infringement Evidence
	 Teardown photograph of processor chip from PS4 Slim.

Exhibit A
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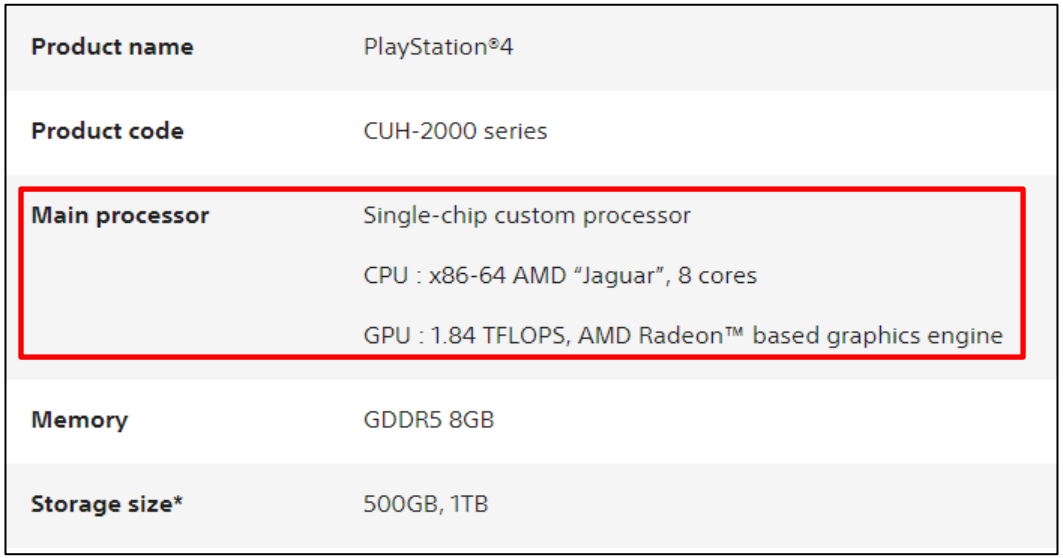
Sony PlayStation 4

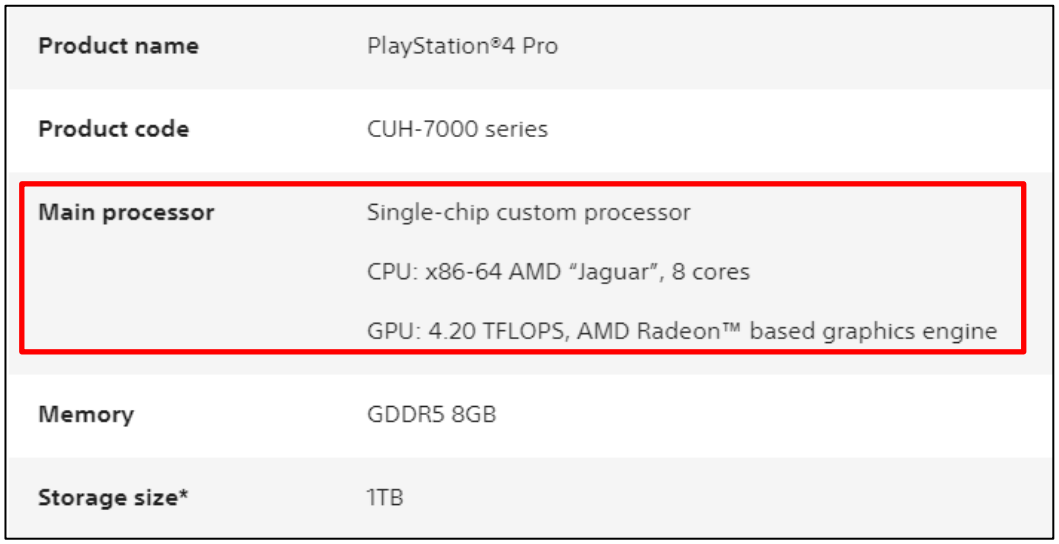
Claim Language	Infringement Evidence
	

Product name	PlayStation®4
Product code	CUH-2000 series
Main processor	Single-chip custom processor CPU : x86-64 AMD "Jaguar", 8 cores GPU : 1.84 TFLOPS, AMD Radeon™ based graphics engine
Memory	GDDR5 8GB
Storage size*	500GB, 1TB

https://www.playstation.com/en-us/ps4/tech-specs/ (regarding PlayStation 4 Slim) (annotations added).

The PlayStation 4 Pro includes a CXD90044GB processor. *See* https://www.techpowerup.com/gpu-specs/playstation-4-pro-gpu.c2876.

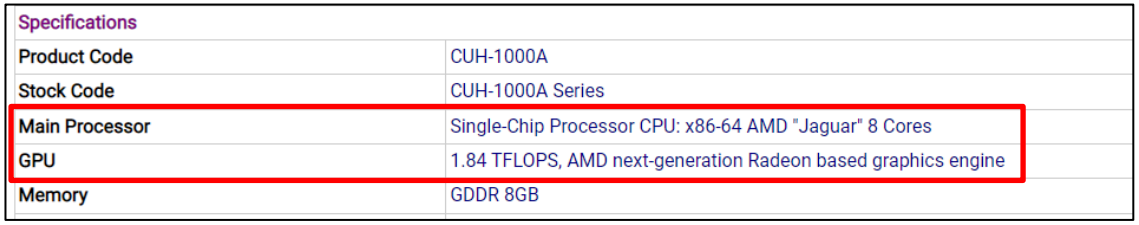
Exhibit A
ACQIS's Preliminary Infringement Contentions for U.S. Patent No. 9,529,768
Sony PlayStation 4

Claim Language	Infringement Evidence
	

Product name	PlayStation®4 Pro
Product code	CUH-7000 series
Main processor	Single-chip custom processor CPU: x86-64 AMD "Jaguar", 8 cores GPU: 4.20 TFLOPS, AMD Radeon™ based graphics engine
Memory	GDDR5 8GB
Storage size*	1TB

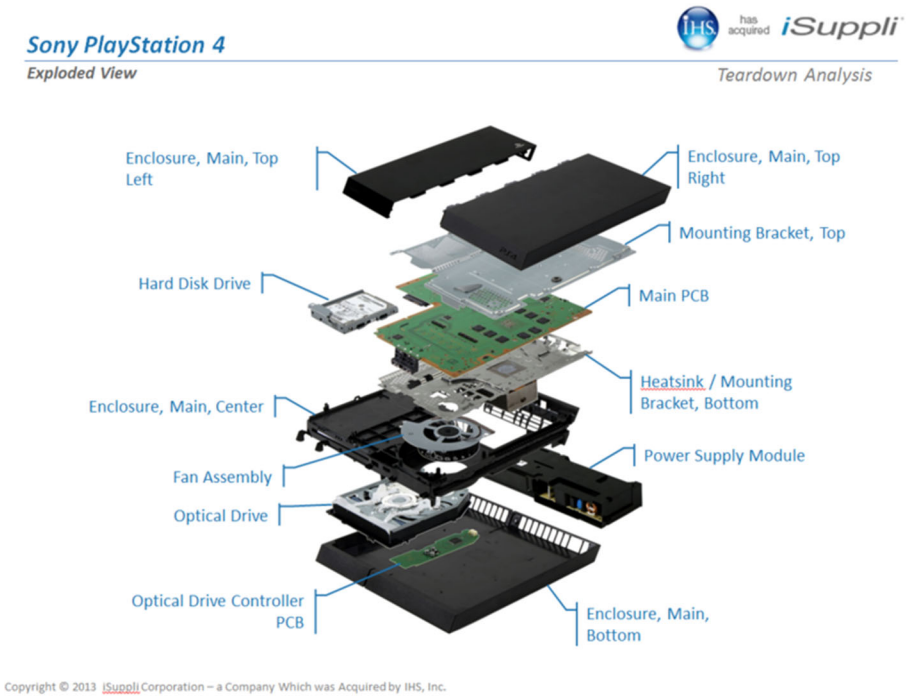
https://www.playstation.com/en-us/ps4/tech-specs/ (regarding PlayStation 4 Pro) (annotations added).

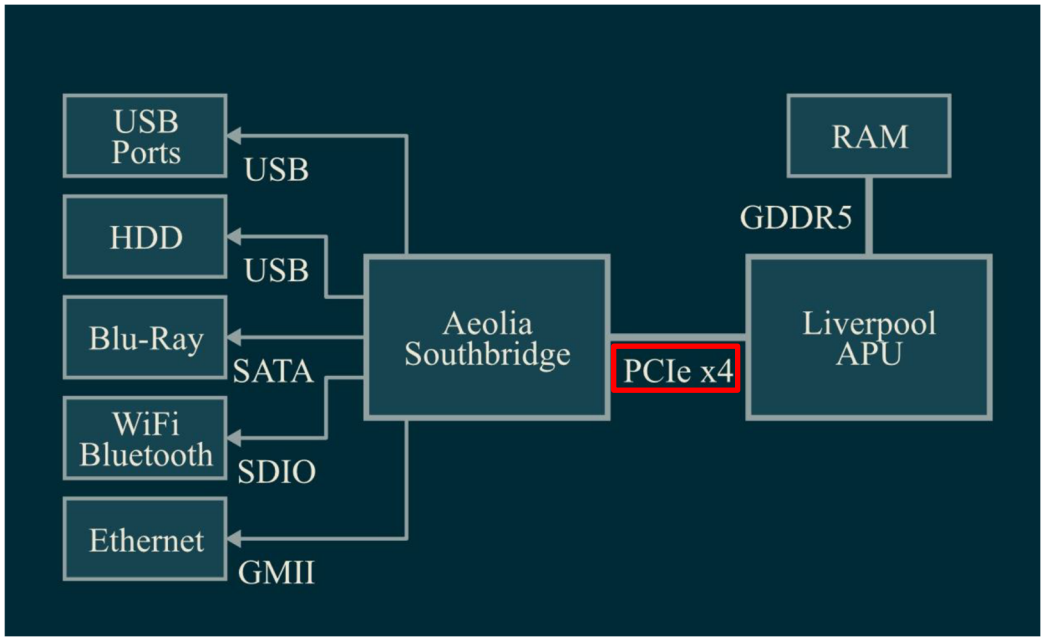
The original PlayStation 4 includes a CXD90026BG processor. *See* https://www.techpowerup.com/gpu-specs/playstation-4-gpu.c2085.

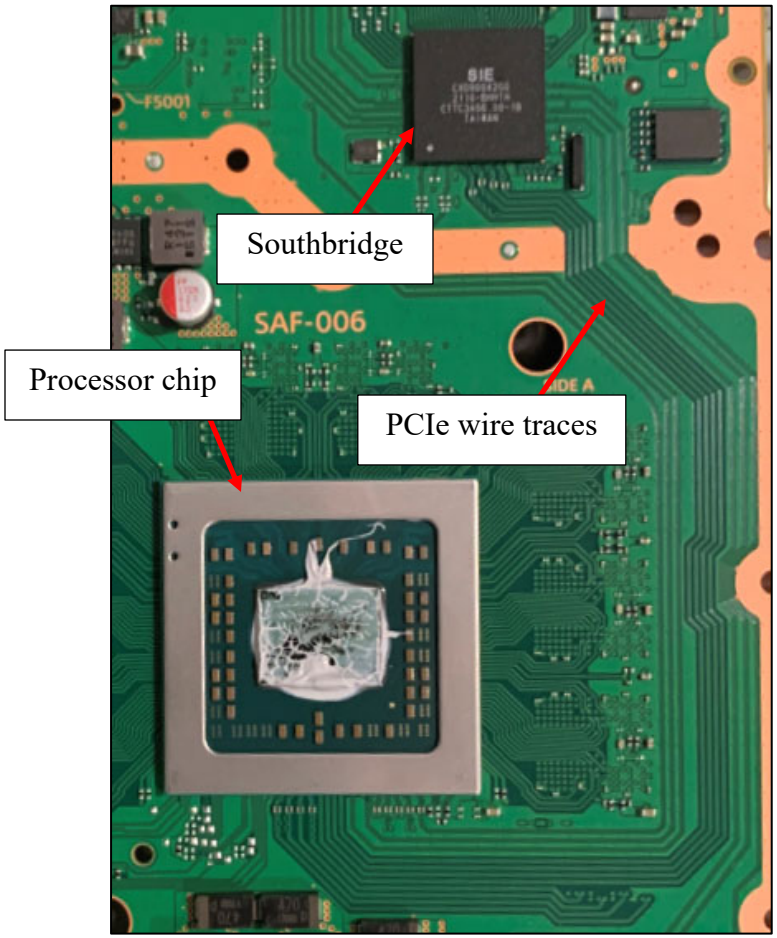


Specifications	
Product Code	CUH-1000A
Stock Code	CUH-1000A Series
Main Processor	Single-Chip Processor CPU: x86-64 AMD "Jaguar" 8 Cores
GPU	1.84 TFLOPS, AMD next-generation Radeon based graphics engine
Memory	GDDR 8GB

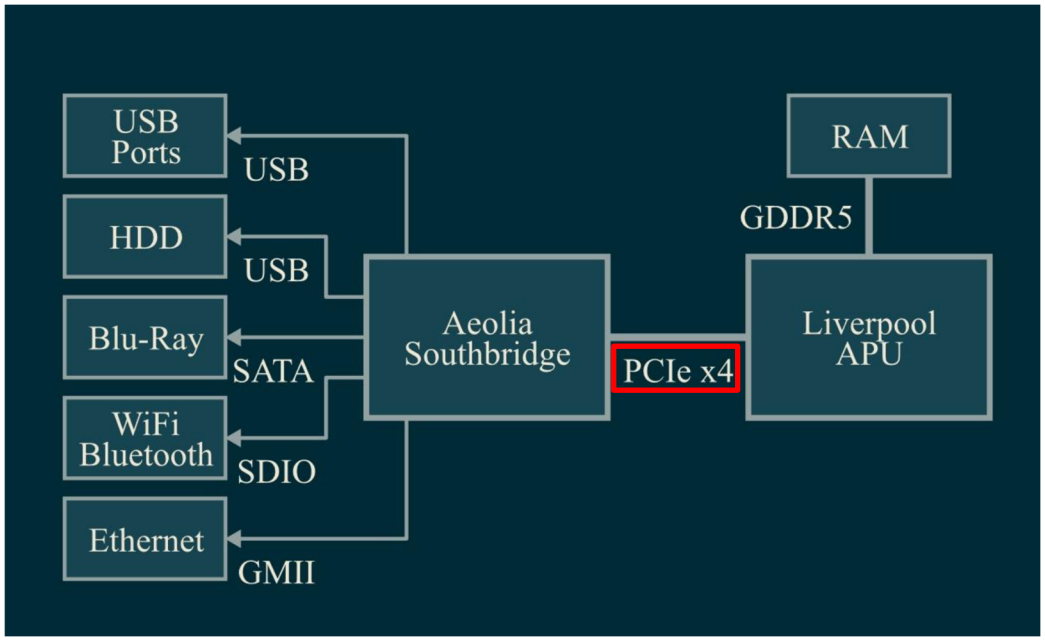
https://www.comx-computers.co.za/CUH-1000A-specifications-110924.htm (regarding PlayStation 4)

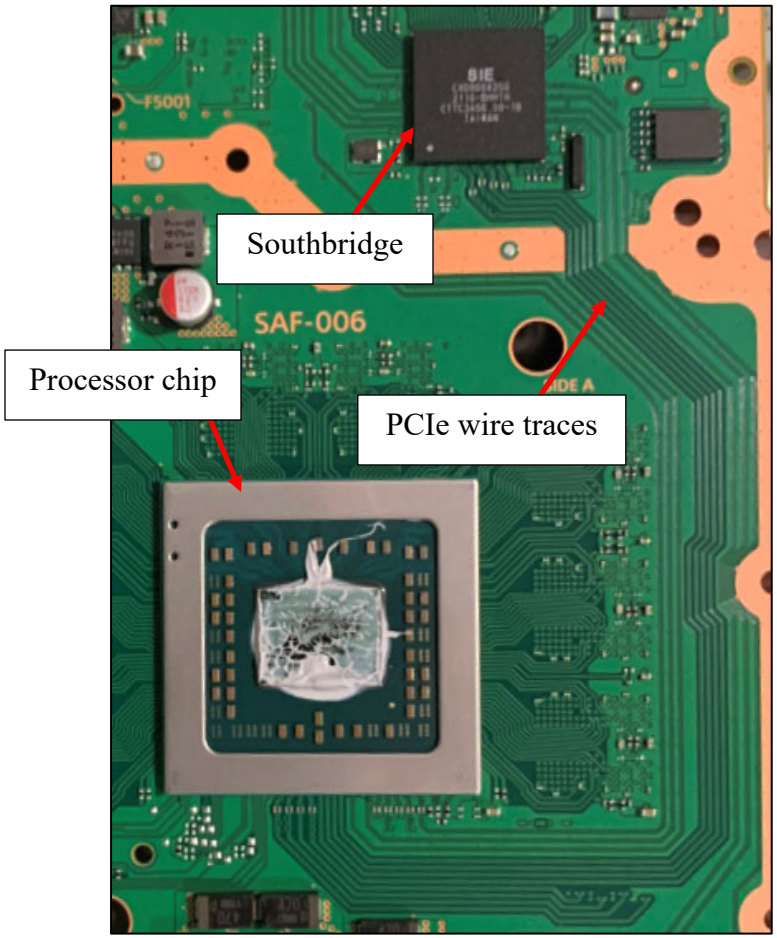
Claim Language	Infringement Evidence
	(annotations added).  https://www.psdevwiki.com/ps4/File:PS4_-_Exploded_View.png. The Sony CXD processor in each PlayStation 4 model contains an integrated central processing unit, interface controller and PLL clock circuitry in a single chip. As shown below, the Sony processor's "Liverpool" APU includes a x4 PCIe interface on-chip.

Claim Language	Infringement Evidence
	 http://www.nextgenupdate.com/forums/ps4-mods-cheats/936464-full-review-ps4-hacking-presentation-ccc-talk-team-fail0verflow.html (annotations added); https://www.youtube.com/watch?v=-AoHGJ1g9aM.

Claim Language	Infringement Evidence
	 Teardown photograph of processor-to-southbridge connection from PS4 Slim (annotations added).

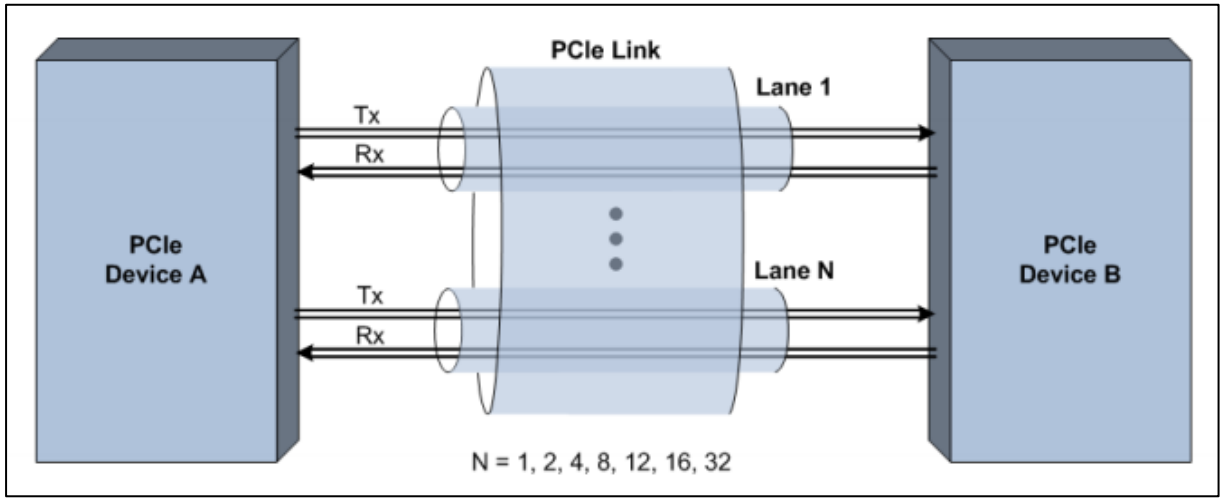
Claim Language	Infringement Evidence
	Because each Sony processor, e.g., the CXD90059GB, supports on-chip PCIe, it necessarily contains one or more logic blocks to implement the PCIe functionality, i.e., a PCIe controller and related circuitry found in the Physical Layer (PHY). This logic block (or plurality of logic blocks) is, and/or is part of, an "interface controller" within the meaning of this limitation. ACQIS does not possess specific information regarding the specific PCIe controller(s) and PHY(s) used in the PlayStation 4 models or their respective Sony processors. ACQIS reserves the right to supplement and/or amend its contentions to provide further specificity based on information obtained in discovery. As discussed below with respect to limitation [1.c], each Sony processor, e.g., the CXD90059GB, includes PLL clock circuitry, including at least in the PHY(s) associated with the PCIe controller(s).
[1.b] a Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller to convey address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in a serial form, wherein the first LVDS channel comprises a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction; and	The Sony CXD processor found in the PlayStation 4, e.g., the CXD90059GB in the PlayStation 4 Slim, which includes an integrated CPU, interface controller and PLL clock circuitry, has a Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller. As discussed above with respect to limitation [1.a], each Sony CXD processor includes a x4 on-chip PCIe interface, as shown below.

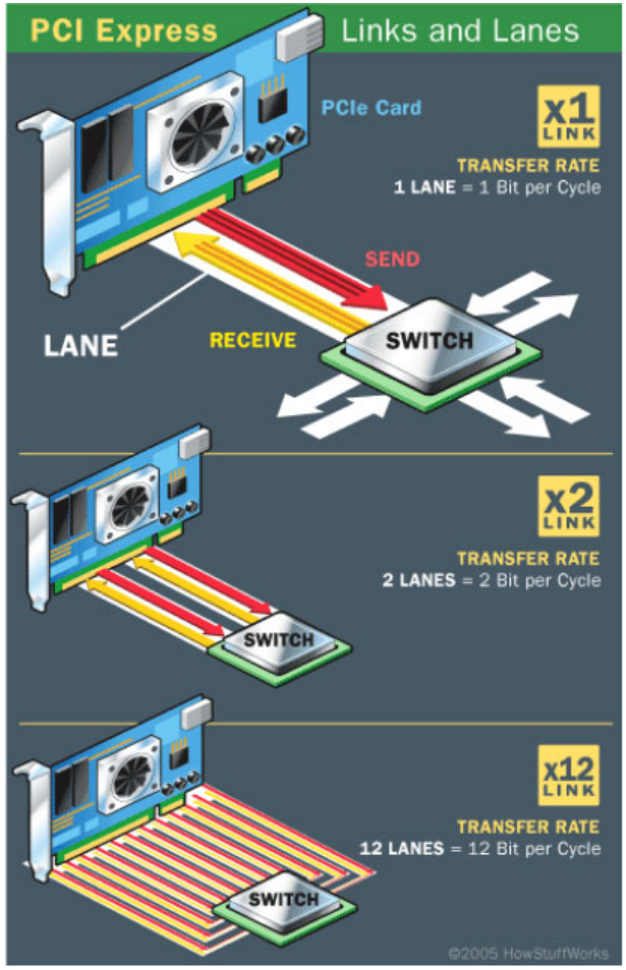
Claim Language	Infringement Evidence
	 http://www.nextgenupdate.com/forums/ps4-mods-cheats/936464-full-review-ps4-hacking-presentation-ccc-talk-team-fail0verflow.html (annotations added); https://www.youtube.com/watch?v=-AoHGJ1g9aM.

Claim Language	Infringement Evidence
	 Teardown photograph of processor-to-southbridge connection from PS4 Slim (annotations added). The PlayStation 4 uses the Sony CXD processor's on-chip PCIe I/O for directly connecting the

Claim Language	Infringement Evidence
	southbridge to the processor chip in a four-lane PCIe configuration, as shown above. The southbridge in the PlayStation 4 Slim is the Sony CXD90042GG, as shown below.  Teardown photograph of southbridge from PS4 Slim. The southbridge chip in each PlayStation 4 model is supplied by Marvell Technology, Inc. *See, e.g.*, https://www.psdevwiki.com/ps4/Southbridge. PlayStation 4 models include various southbridge models, including CXD90025G ("Aeolia"), CXD90036G ("Belize"), CXD90042GG ("Baikal"), and CXD90046GG ("Belize 2"). *Id.* The functionality of each unique southbridge is identical in relevant part. The PCIe interface used in the PlayStation 4 for connecting the southbridge to the CPU, as described

Claim Language	Infringement Evidence
	above, has an LVDS channel directly extending from the interface controller that conveys address and data bits of a PCI bus transaction in a serial form. As discussed above with respect to limitation [1.a], each Sony CXD processor contains one or more logic blocks to implement the PCIe functionality, i.e., a PCIe controller and related circuitry found in the Physical Layer (PHY). The PCIe controller has an associated PHY connected to it via the PIPE interface. ACQIS does not possess specific information regarding the specific PCIe controller(s) and PHY(s) used in the PlayStation 4 or in each Sony CXD processor. ACQIS reserves the right to supplement and/or amend its contentions to provide further specificity based on information obtained in discovery. LVDS is central to PCIe, providing the physical transmission medium, and all implementations of PCIe utilize LVDS: > PCI Express . . . is a serial bus which uses two low-voltage differential LVDS pairs, at 2.5Gb/s in each direction [one transmit, and one receive pair]. A PCI Express link is comprised of these two unidirectional differential pairs each operating at 2.5Gbps to achieve a basic [overall] throughput of 5Gbps [before accounting for over-head]. http://www.interfacebus.com/PCI-Express-Bus-PCIe-Description.html. This LVDS channel comprises a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction. As shown in the exemplary PCIe illustrations below, each lane in a PCIe implementation contains a first unidirectional, differential signal pair to convey data in a first direction (i.e., the Tx pairs in the upper illustration and the signal pairs in red in the lower illustration) and a second unidirectional, differential signal pair to convey data in a second direction (i.e., the Rx signal pairs in the upper illustration and the signal pairs in yellow in the lower illustration). In a multi-lane PCIe configuration, the stream of bytes that make up a TLP go through byte striping, which distributes the

Claim Language	Infringement Evidence
	bytes across the available lanes for serialization. *See* PCI Express Base Specification, Revision 3.0 (Nov. 10, 2010) at 195-198. The transaction's byte-oriented data (character) is encoded, serialized, and output one byte at a time per lane in the PCIe link. *Id.* Thus in PCIe, the TLP is in serial form for all link widths. *Id.*  *Silicon Labs AN562, PCI Express 3.1 Jitter Requirements* (Rev. 0.2 11/15) (available at https://www.silabs.com/documents/public/application-notes/AN562.pdf), at 2.

Claim Language	Infringement Evidence
	 https://computer.howstuffworks.com/pci-express.htm.

Claim Language	Infringement Evidence
	The data that is transmitted in a serial PCIe bus transaction includes address and data bits of a PCI bus transaction. The transaction layer packets (TLPs) used for PCIe data transmission include both address and data bits of a PCI bus transaction. **The Address Element** The address elements of the TLP provide the address to select specific bytes within the memory and I/O address spaces. The address elements also provide the ID Routing and the register address to select the specific bytes of the configuration register block in the configuration address space. Finally, address elements also provide the ID and Implied Routing for the message address space. *Header field of TLP contains:* **ADDRESS:** The "typical" address bits for memory and I/O address space. The address can also be used in message vendor-defined transaction packets. *The Complete PCI Express Reference*, Intel Press (2003), at 218. **The Data Element** The data element of the transaction packet provides the actual data being accessed. *The Complete PCI Express Reference*, Intel Press (2003), at 220.

Claim Language	Infringement Evidence

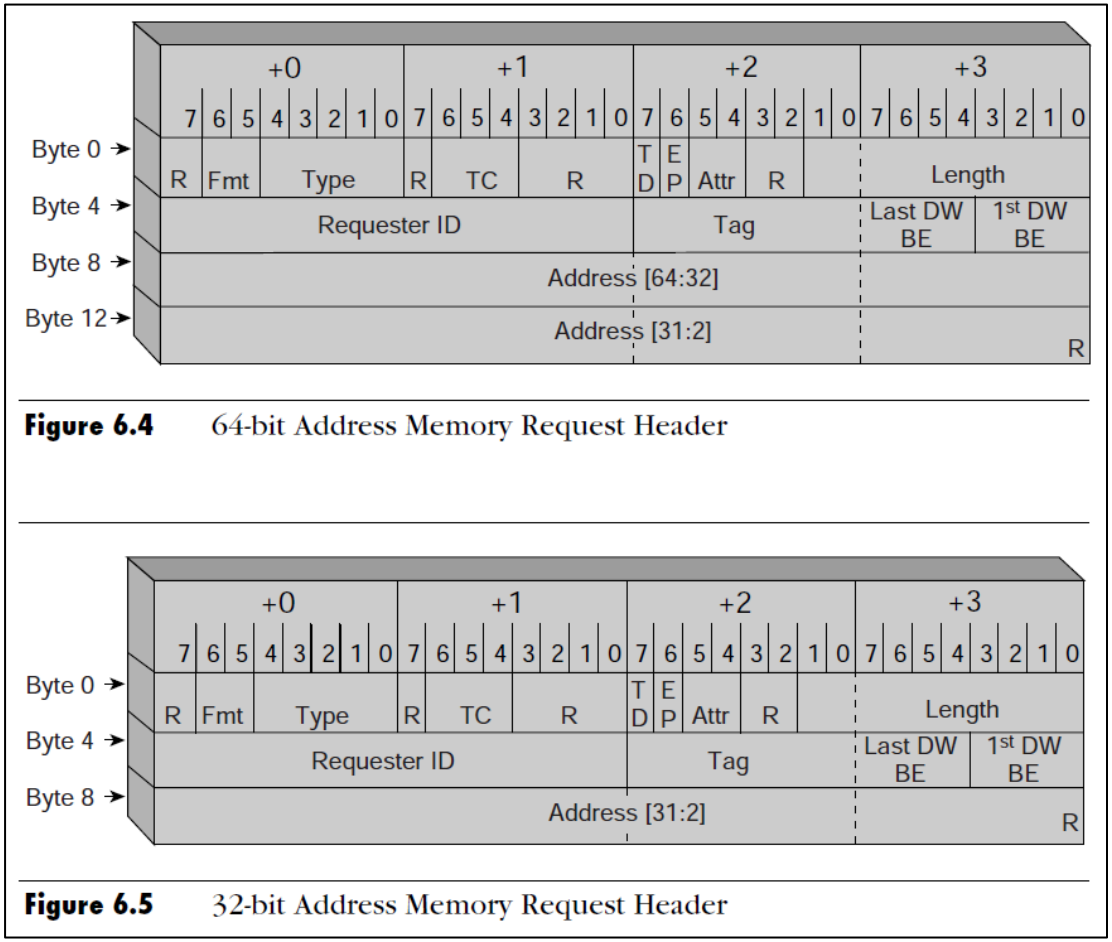


Figure 6.4 64-bit Address Memory Request Header

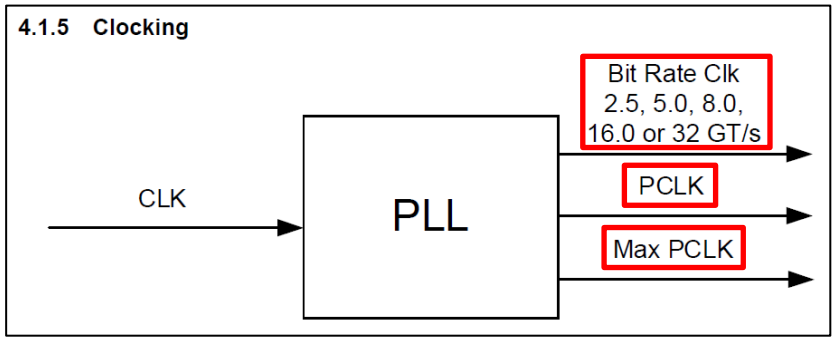
Figure 6.5 32-bit Address Memory Request Header

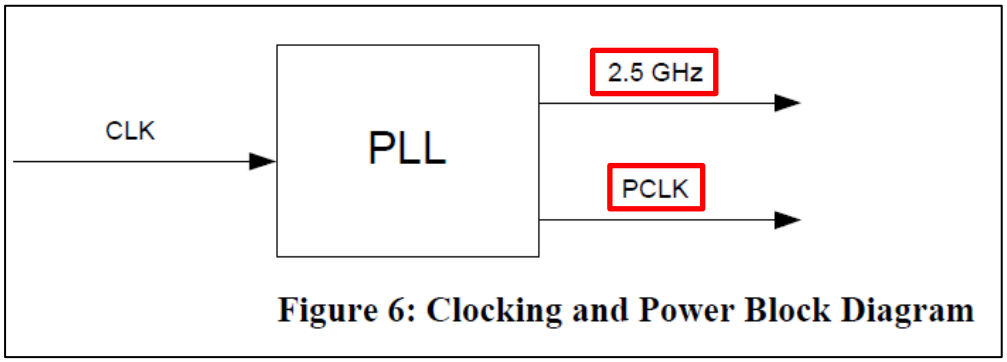
Introduction to PCI Express – A Hardware and Software Developers Guide, Intel Press (2003), at 100.

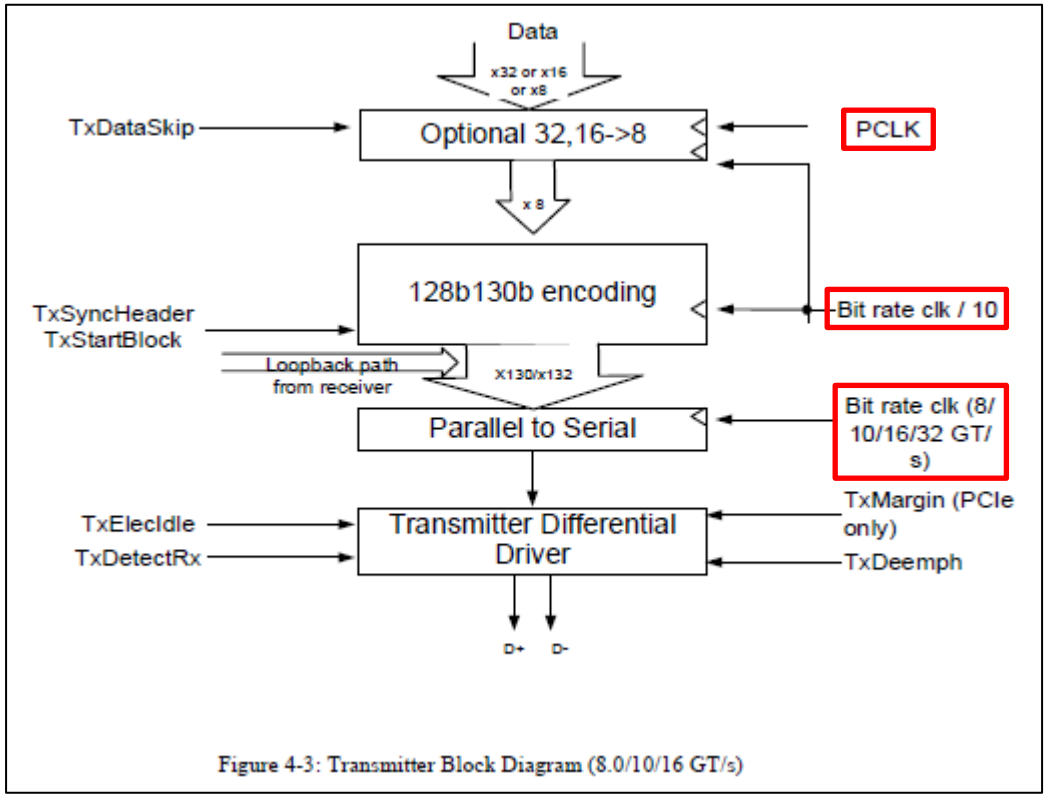
Claim Language	Infringement Evidence
	Further, PCIe is backwards compatible with PCI, as PCI is described in the PCI Local Bus Specification. In PCIe, "[k]ey PCI attributes, such as its usage model, load-store architecture, and software interfaces, are maintained, whereas its parallel bus implementation is replaced by a highly scalable, fully serial interface." PCI Express Base Specification, Revision 3.0 (Nov. 10, 2010) ("PCIe 3.0 Spec.") at 37. PCIe maintains a "PCI compatible software model," providing: ❑ **PCI compatible software model:** • Ability to enumerate and configure PCI Express hardware using PCI system configuration software implementations with no modifications • Ability to boot existing operating systems with no modifications • Ability to support existing I/O device drivers with no modifications • Ability to configure/enable new PCI Express functionality by adopting the PCI configuration paradigm PCIe 3.0 Spec. at 38. A Peripheral Component Interconnect (PCI) bus transaction, in accordance with the industry standard PCI Local Bus Specification, Revision 2.2 (Dec. 18, 1998) ("*PCI Specification*"), for communication with an interconnected peripheral component (a "PCI transaction") consists of an address phase and one or more data phases. (*See, e.g.*, *PCI Specification* at 9, 301.) Example transactions include input/output (I/O) read, I/O write, memory read, memory write, configuration read, and configuration write. (*See, e.g.*, *PCI Specification* at 21-23.) A PCI transaction facilitates communication and data transfer among computer components, such as processors, memory, and peripheral devices. (*See, e.g.*, *PCI Specification* at 1, 3.) PCI transactions include a set of address bits, a set of data bits, a set of command bits, and a set of byte enable information bits. (*See, e.g.*, *PCI Specification* at 9-10.) The

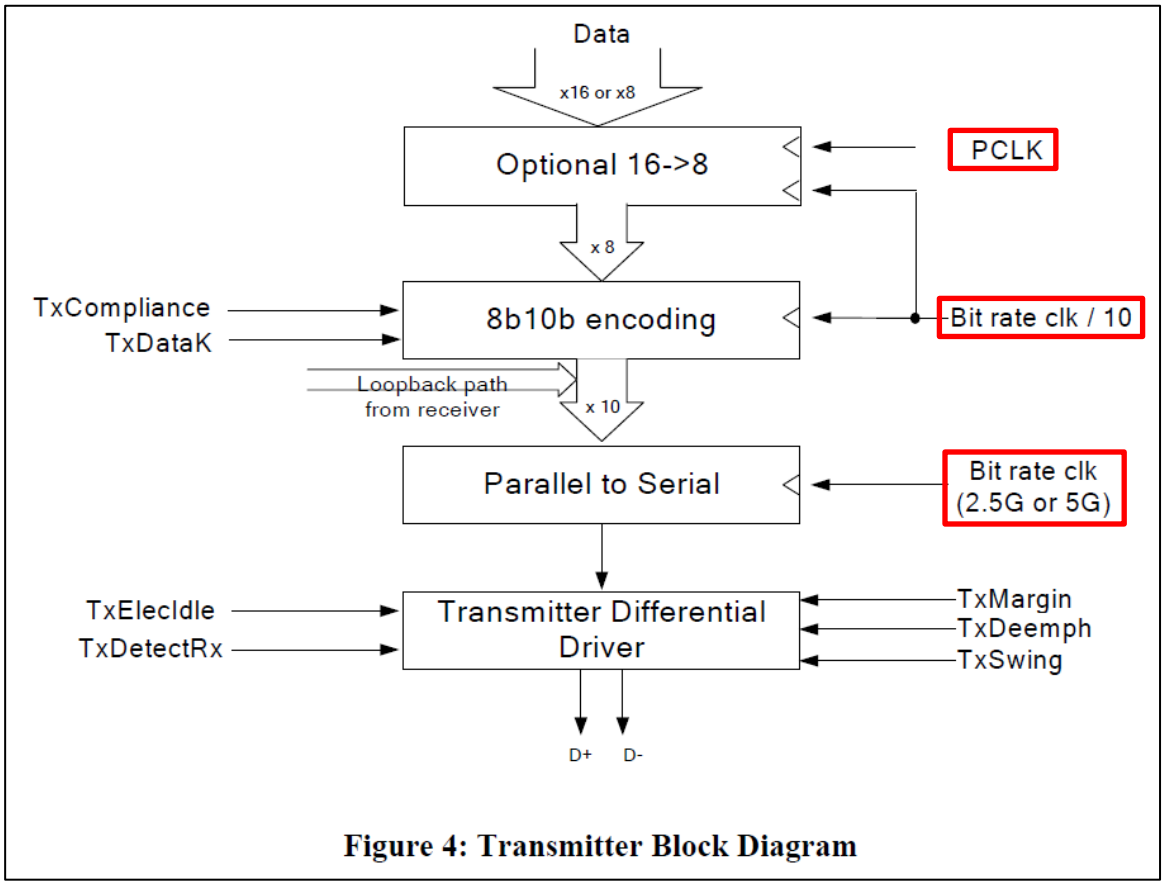
Claim Language	Infringement Evidence
	address bits allow one component to communicate with another specific component. (*See, e.g.*, *PCI Specification* at 9, 27-29.) The data bits transfer data from one component to another. (*See, e.g.*, *PCI Specification* at 9.) The command bits indicate the type of transaction (such as memory, I/O, or configuration) and control the transaction. (*See, e.g.*, *PCI Specification* at 21-24.) The byte enable information bits indicate the size of the data transfer and the bytes in the data transfer that contain valid data. (*See, e.g.*, *PCI Specification* at 10, 28.) The PCI Express™ (PCIe) Base Specification Revision 1.0a (Apr. 15, 2003) ("*PCIe Specification*"), utilizes transactions to facilitate communication and data transfer among computer components. (*See, e.g.*, *PCIe Specification* at 27.) PCIe transactions are defined in the PCIe Transaction Layer. (*See, e.g.*, *PCIe Specification* at 36.) PCIe transactions include read and write transactions. (*See, e.g.*, *PCIe Specification* at 42.) PCIe transactions are communicated using bits. (*See, e.g.*, *PCIe Specification* at 44.) PCIe employs the three transaction types (memory, I/O, and configuration) described in the PCI Local Bus Specification. (*See, e.g.*, *PCIe Specification* at 36, 45.) PCIe provides a PCI-compatible software model. (*See, e.g.*, *PCIe Specification* at 27.) PCIe transactions include command bits to indicate the type of transaction (such as memory, I/O, or configuration) and control the transaction. (*See, e.g.*, *PCIe Specification* at 44-47.) PCIe transactions include address bits to allow one component to communicate with another specific component. (*See, e.g.*, *PCIe Specification* at 49-50; *see also, e.g.*, *The Complete PCI Express Reference*, Intel Press (2003), at 218.) PCIe transactions include data bits to transfer data between components. (*See, e.g.*, *PCIe Specification* at 44; *see also, e.g.*, *The Complete PCI Express Reference*, Intel Press (2003), at 220.) PCIe transactions include byte enable information to indicate the size of the data transfer and the bytes in the data transfer that contain valid data. (*See, e.g.*, *PCIe Specification* at 52-53; *see also, e.g.*, *Introduction to PCI Express – A Hardware and Software Developers Guide*, Intel Press (2003), at 100.) A PCIe transaction therefore provides a Peripheral Component Interconnect (PCI) bus transaction in accordance with the industry standard PCI Local Bus Specification, for communication with an

Claim Language	Infringement Evidence
	interconnected peripheral component. A PCIe transaction provides address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction. To the extent that Sony contends that a PCIe transaction does not provide a Peripheral Component Interconnect (PCI) bus transaction or address bits, data bits, and/or byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction, a PCIe transaction satisfies these claim elements under the doctrine of equivalents. A PCIe transaction—including its address, data, and byte enable information bits—performs substantially the same function, in substantially the same way, to obtain the same result as a PCI transaction, including its address, data, and byte enable information bits. A PCIe transaction—including its address, data, and byte enable information bits—is not substantially different from a PCI transaction, including its address, data, and byte enable information bits. A PCI transaction and a PCIe transaction both perform the function of facilitating communication among components in a computer system. A PCI transaction and a PCIe transaction perform this function by utilizing address bits, data bits, and byte enable bits. In both PCI and PCIe transactions, address bits allow one component to communicate with another specific component. In both PCI and PCIe transactions, data bits transfer data from one component to another. In both PCI and PCIe transactions, command bits indicate the type of transaction and control the transaction. In both PCI and PCIe transactions, byte enable bits indicate the size of the data transfer and the bytes in the data transfer that contain valid data. A PCI transaction and a PCIe transaction therefore both perform the function of facilitating communication among components in a computer system in substantially the same way. The address bits, data bits, command bits, and byte enable information bits in a PCIe transaction do not differ substantially from the address bits, data bits, command bits, and byte enable information bits in a PCI transaction. A PCIe transaction uses substantially similar bits as a PCI transaction in order to maintain consistency and software compatibility with PCI. A PCI transaction and a PCIe transaction produce the same result of communication among components in a computer system.

Claim Language	Infringement Evidence
[1.c] wherein the PLL clock circuitry generates different clock frequencies, and the interface controller conveys the PCI bus transaction through the LVDS channel based on the different clock frequencies.	As discussed above with respect to limitation [1.a], the processor in the PlayStation 4, i.e., each Sony CXD processor, includes an on-chip PCIe controller and an associated PHY. The PHY in each Sony CXD processor, e.g., the CXD90059GB processor in the PlayStation 4 Slim, includes PLL clock circuitry. The PHY contains at least one PLL and likely contains multiple PLLs. Within the PHY Interface for the PCI Express Architecture (PIPE), the PLL clock circuitry generates at least two clocks at different frequencies. One frequency is used as a bitrate clock (2.5 GHz – 32 GHz, depending on the PCIe transfer rates supported; PCIe 3.x supports 8 GT/s, and PCIe 2.x supports 5 GT/s), and the other is for the PIPE interface to the rest of the PCIe controller, i.e., PCLK (or pipe_clock) at 125 MHz or 250 MHz. Additionally, the PLL clock circuitry may generate a third clock frequency which is the bitrate clock divided by 10, i.e., bit rate clk / 10. Thus, the PLL clock circuitry generates different clock frequencies, which are used to convey the PCI bus transactions through the LVDS channel.  *PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort, and Converged IO Architectures*, Version 5.1 (2018) (available at https://www.intel.com/content/dam/www/public/us/en/documents /white-papers/phy-interface-pci-express-sata-usb30-architectures-3.1.pdf), at 32 (annotations added).

Claim Language	Infringement Evidence
	 **Figure 6: Clocking and Power Block Diagram** *PHY Interface for the PCI Express Architecture*, Version 2.00 (2007) (available at http://www.applistar.com/wp-content/uploads/apps/pipe2_00.pdf), at 11 (annotations added).

Claim Language	Infringement Evidence
	 Figure 4-3: Transmitter Block Diagram (8.0/10/16 GT/s) *PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort, and Converged IO Architectures*, Version 5.1 (2018) (available at https://www.intel.com/content/dam/www/public/us/en/documents /white-papers/phy-interface-pci-express-sata-usb30-architectures-3.1.pdf), at 29 (annotations added).

Claim Language	Infringement Evidence
	 **Figure 4: Transmitter Block Diagram** *PHY Interface for the PCI Express Architecture*, Version 2.00 (2007) (available at http://www.applistar.com/wp-content/uploads/apps/pipe2_00.pdf), at 10 (annotations added).

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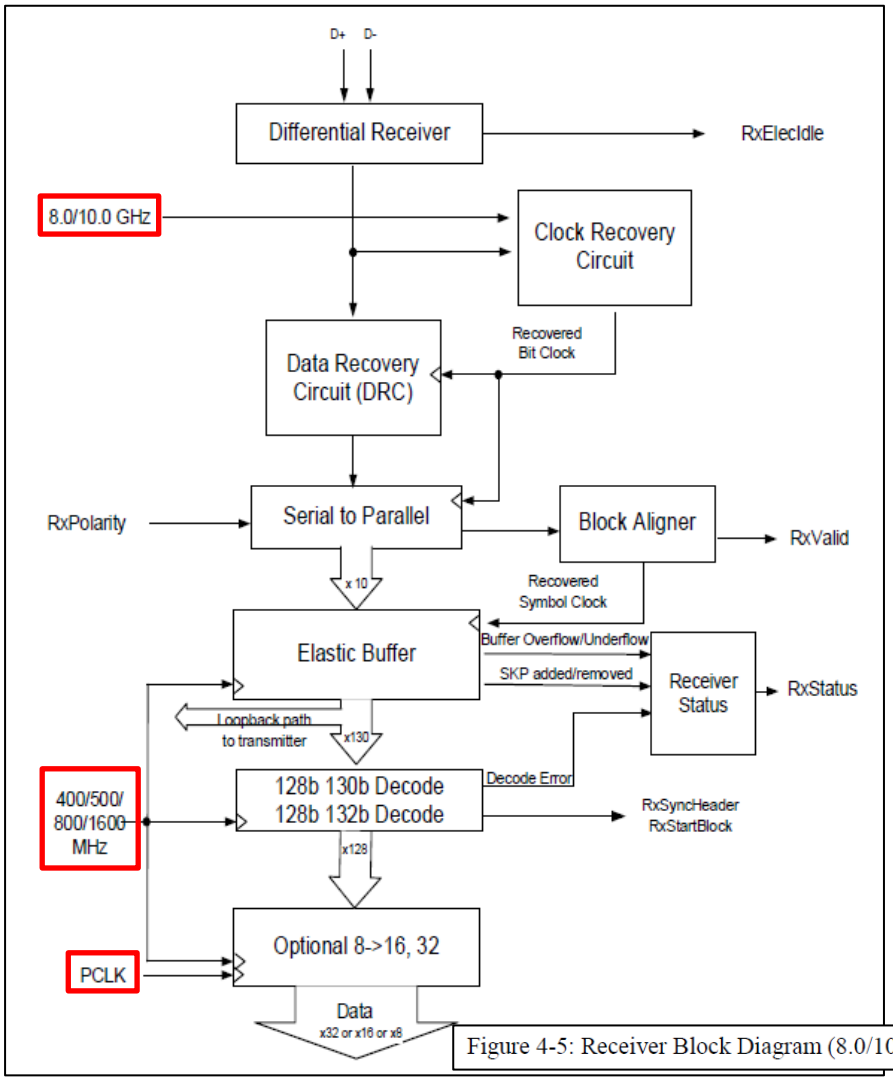
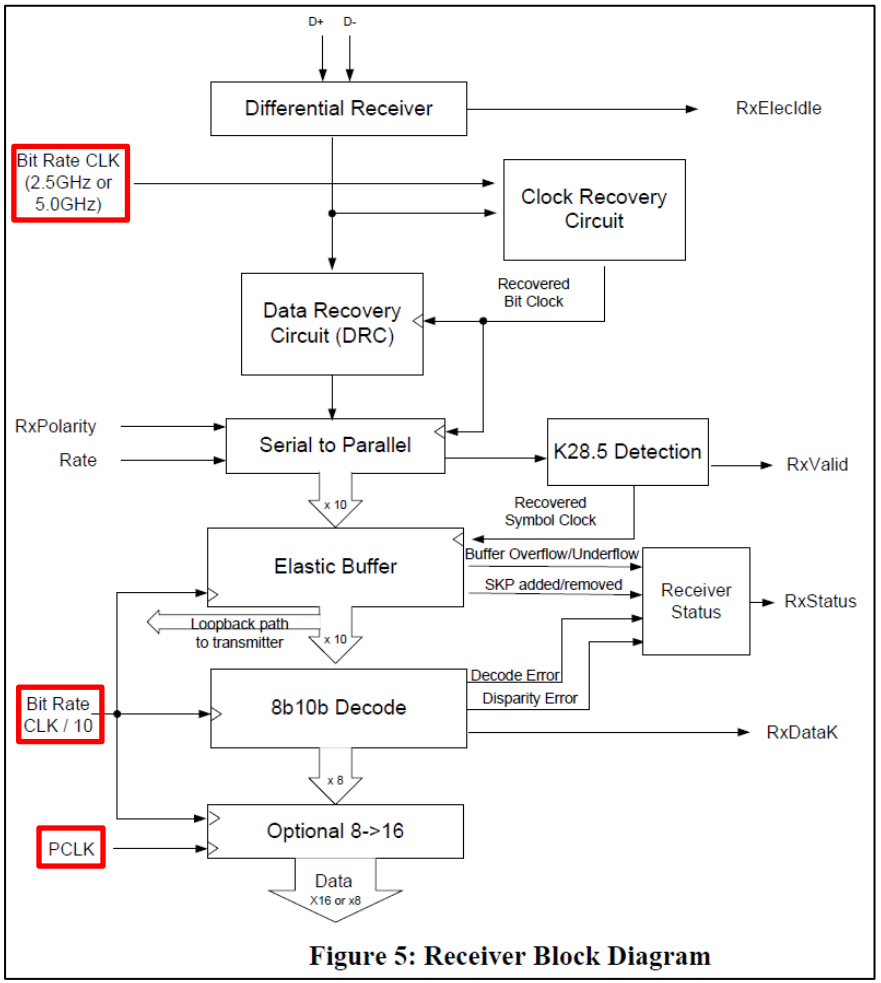
Claim Language	Infringement Evidence
	 Figure 4-5: Receiver Block Diagram (8.0/10/16 GT/s)

Claim Language	Infringement Evidence
	PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort, and Converged IO Architectures, Version 5.1 (2018) (available at https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/phy-interface-pci-express-sata-usb30-architectures-3.1.pdf), at 31-32 (annotations added).

Exhibit A
ACQIS's Preliminary Infringement Contentions for U.S. Patent No. 9,529,768
Sony PlayStation 4

Claim Language	Infringement Evidence
	 **Figure 5: Receiver Block Diagram**

<table>
<tr><th>Claim Language</th><th>Infringement Evidence</th></tr>
<tr><td></td><td>

PHY Interface for the PCI Express Architecture, Version 2.00 (2007) (available at http://www.applistar.com/wp-content/uploads/apps/pipe2_00.pdf), at 11 (annotations added).

Table 6-18. External Input Signals

Name	Active Level	Description	Relevant Protocols
CLK	Edge	This differential Input is used to generate the bit-rate clock for the PHY transmitter and receiver. Specs for this clock signal (frequency, jitter, …) are implementation dependent and must be specified for each implementation. This clock may have a spread spectrum modulation.	PCIe, SATA, USB, DisplayPort, Converged IO
PCLK	Rising Edge	*This signal is relevant for "PCLK as PHY Input" mode only.* All data movement across the parallel interface is synchronized to this clock. This clock operates at a frequency set by *PCLK Rate*. The rising edge of the clock is the reference for all signals. Spread spectrum modulation on this clock is allowed.	PCIe, SATA, USB, DisplayPort, Converged IO

PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort, and Converged IO Architectures, Version 5.1 (2018) (available at https://www.intel.com/content/dam/www/public/us/en/documents /white-papers/phy-interface-pci-express-sata-usb30-architectures-3.1.pdf), at 77.

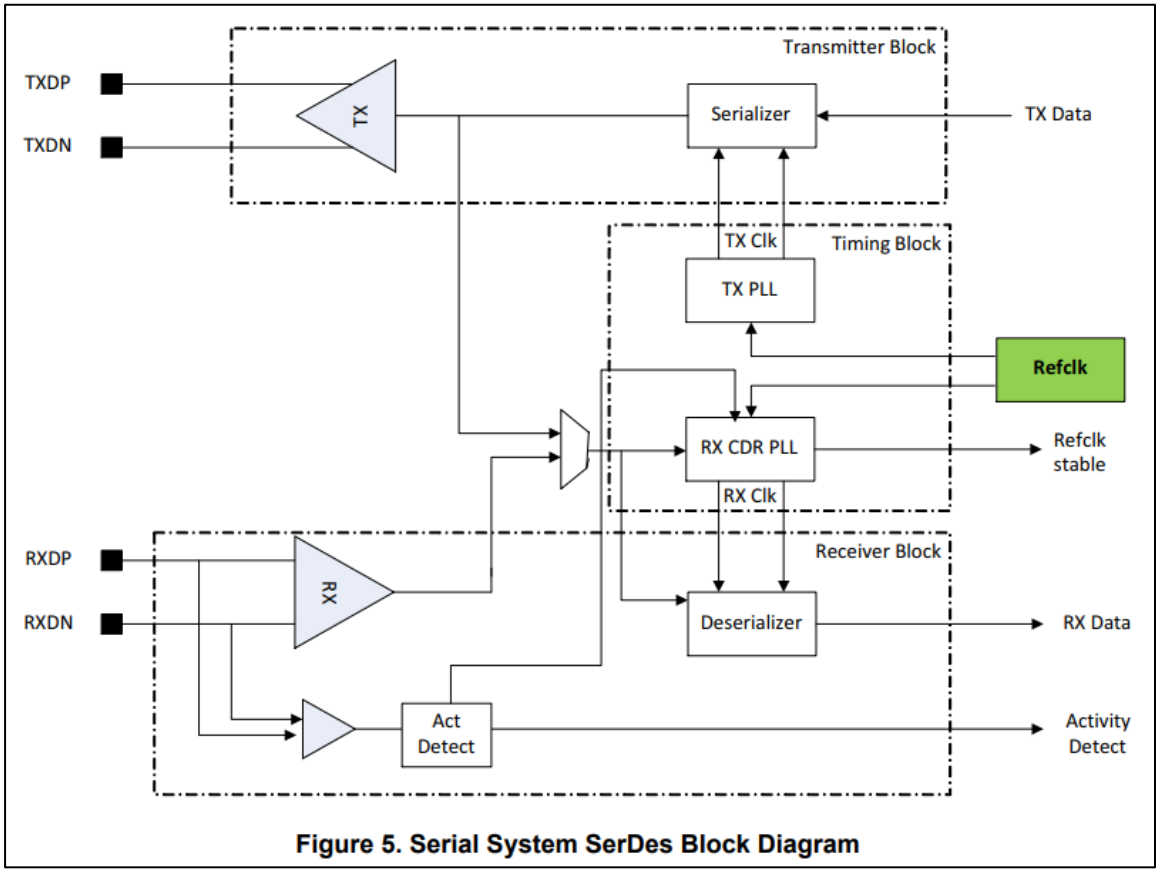
</td></tr>
</table>

Claim Language	Infringement Evidence

Name	Direction	Active Level	Description
CLK	Input	Edge	This Input is used to generate the bit-rate clock for the PHY transmitter and receiver. Specs for this clock signal (frequency, jitter, …) are implementation dependent and must be specified for each implementation. This clock may have a spread spectrum modulation.
PCLK	Output	Rising Edge	Parallel interface data clock. All data movement across the parallel interface is synchronized to this clock. This clock operates at 125MHz, 250MHz, or 500 MHz depending on the *Rate* control input and the data interface width. The rising edge of the clock is the reference for all signals. Spread spectrum modulation on this clock is allowed.

PHY Interface for the PCI Express Architecture, Version 2.00 (2007) (available at http://www.applistar.com/wp-content/uploads/apps/pipe2_00.pdf), at 16.

Additionally, PLLs are often used within the PCIe PHY as part of the clock and data recovery (CDR) functionality of the receiver.

Claim Language	Infringement Evidence
	 **Figure 5. Serial System SerDes Block Diagram** *A System Designer's Guide for Building a PCIe Clock Tree while Addressing Timing Challenges*, Application Note AND9202/D, ON Semiconductor (available at https://www.onsemi.com/pub/Collateral/AND9202-D.PDF), at 5.

Claim Language	Infringement Evidence
	The PLL clock circuitry in the PCIe PHY in each Sony CXD processor also generates different clock frequencies based on PCIe version and the associated data transfer rate. The PLL clock circuitry, e.g., the transmit (TX) PLL, multiplies the reference clock frequency to achieve the desired data rate. This standard approach is consistent with the discussion below. **3. Refclk and Clocking Architectures** An external clock reference clock (Refclk) is required for transmitting data between two PCIe devices. A Refclk frequency of 100 MHz ±300 ppm is specified for all three line rates (2.5 Gbps, 5.0 Gbps, 8.0 Gbps). The burden has been placed on the TX PLL to multiply the 100 MHz Refclk frequency to the desired data rate. Although the Refclk frequency has remained the same, the jitter performance requirements of the Refclk have improved to support the higher data rates prevalent with PCI Express 2.1 and 3.1. We will look at the Refclk jitter requirements in the following sections. *Silicon Labs AN562, PCI Express 3.1 Jitter Requirements* (Rev. 0.2 11/15) (available at https://www.silabs.com/documents/public/application-notes/AN562.pdf), at 3. The interface controller in each Sony CXD processor, e.g., the CXD90059GB processor in the PlayStation 4 Slim, thus conveys the PCI bus transaction through the LVDS channel based on different clock frequencies.
2. The computer of claim 1 wherein the interface controller conveys the PCI bus transaction through the LVDS channel based on a selected frequency of the different clock frequencies.	*See* claim 1, above. The interface controller in each Sony CXD processor in the PlayStation 4, e.g., the CXD90059GB processor in the PlayStation 4 Slim, conveys the PCI bus transaction through the LVDS channel based on a selected frequency of the different clock frequencies. The PLL within the PCIe PHY will select one bit rate frequency based on the version of the PCIe protocol and the highest common data rate used for the link.